What is claimed is:

1. A master slice semiconductor integrated circuit, comprising:

at least two wiring layers for wirings; and

a plurality of clock buffers connected by clock wirings in the form of a clock tree having at least two cascaded stages to distribute clock signals to a plurality of sequential circuits;

wherein said clock wiring among said clock buffers comprises a wiring layer switching portion which switches a wiring layer from a lower wiring layer of said at least two wiring layers to an upper wiring layer of said at least two wiring layers and then switches from said upper wiring layer to said lower wiring layer.

2. The master slice semiconductor integrated circuit according to claims 1, wherein said wiring layer switching portion comprises a via wiring connecting said clock wiring formed of said lower wiring layer and said clock wiring formed of said upper wiring layer.

3. The master slice semiconductor integrated circuit according to claims 1, wherein said clock buffers are selectors, and said selectors comprise a multiplexer which select and outputs a clock signal from a plurality of clock signals.

4. The master slice semiconductor integrated circuit according to claim 1,

wherein said wiring layer switching portion comprises:

an output wiring which is formed of said lower wiring layer and connects one end thereof to the clock output of the clock buffer of a former stage;

an output side via wiring which connects one end thereof to the other end of said output wiring and connects the other end thereof to said upper wiring layer;

an input wiring which is formed of said lower wiring layer and connects one end thereof to the clock input of the clock buffer of a later stage; and

an input side via wiring which connects one end thereof to the other end of said input wiring and connects the other end thereof to said upper wiring layer; and

wherein said upper wiring layer is a wiring layer for customized wirings, and said lower wiring layer is a wiring layer for fixed wirings.

5. The master slice semiconductor integrated circuit according to claim 4, further comprising a wiring which is formed of said upper wiring layer and connects the other end of said output side via wiring and the other end of said input side via wiring.

6. The master slice semiconductor integrated circuit according to claim 4, further comprising a wiring which is formed of said upper wiring layer and connects the other end of said input side via wiring and a fixed voltage source.

7. The master slice semiconductor integrated circuit according to claim 4, further comprising a wiring which is formed of said upper wiring layer and connects an output of a circuit other than said clock buffers and the other end of said input side via wiring.

8. The master slice semiconductor integrated circuit according to claim 4, further comprising a wiring which is formed of said upper wiring layer and connects an output of a circuit other than said clock buffers and the other end of said output side via wiring.

9. The master slice semiconductor integrated circuit according to claims 4, further comprising a wiring which has a dummy load capacity equivalent to a load capacity connected to said input side via wiring, and is formed of said upper wiring layer and connected to the other end of said output side via wiring.

10. A wafer for master slice for manufacturing the master slice semiconductor integrated circuit according to claim 1.